

Hi-Res Static Screen Ram Schematics Overview
By Michael Matte
September 20, 2019

Subject: Re: Hi-Res Static RAM Project Update
From: MCM Design
Date: 9/20/2019, 5:37 PM
To: Adam Trionfo

The DWGs 1 thru 6 are finalized. You can post/forward these first 6 drawings as desired. DWG 5 as shown is for hi-res operation only with no multi-paging. The upcoming, additional drawings will be submitted to you as options to the original hi-res static screen RAM scheme (DWG 5). A user interested in building the new hi-res static screen RAM scheme can choose what option he/she wants to add on. There WILL be an option drawing for someone that just wants to operate the static screen RAM in low or hi-res with NO multi-paging. An option drawing will include and indicate any rewire necessary to DWG 4 or 5.

I just finished writing my overview. I will send it to you in a few minutes after I proof read it.

Bye.
MCM

Subject: Hi-Res Static RAM Project Update
From: MCM Design
Date: 9/20/2019, 5:54 PM

HI-RES STATIC SCREEN RAM SCHEMATICS OVERVIEW

DWG 1
Modified Hi-Res Motherboard, Mounted 28 Pin Socket Wiring
Details the necessary motherboard modifications for hi-res operation. Includes 28 wiring lines from the motherboard to the 28 pin WW socket mounted on the motherboard.

DWG 2
Bally Motherboard To Hi-Res Screen RAM Board
Shows some of the necessary interfacing from the 28 pin ribbon cable connection on the motherboard to the static screen RAM board scheme and the TV display scan circuitry detailed in DWG 5.

DWG 3
Bally Motherboard To Hi-Res Screen RAM Board
Shows additional interfacing and timing circuitry. Reference above DWG 2 description.

DWG 4
74LS138 Enabler Decoder
Details the 74LS138 decoder for proper operation of the Z80 screen RAM read/write data bus and the TV display scan 32 bit read (scan) data bus.

DWG 5

Static Screen RAM Interfacing

Details interfacing and all connections to the 4 banks of static screen RAM. Includes connections to the four 74LS166 TV display scan serial shifter chips.

User Notes

1. Check your static RAM pin layout for compatibility with the static RAM pin layout in DWG 5. If your static RAM pin layout is NOT compatible, wire your RAM to suit proper operation (or purchase compatible chips) and revise your version of DWG 5 for future reference.

2. DWG 5 as shown is wired for hi-res operation only with no multi-paging. To manually run this DWG 5 scheme in low-res, remove the IC12 chip 74LS138 from its socket. Add a jumper wire from the socket pin 15 to gnd pin 8. This jumper enables the Bank 0 RAM data bus for low-res operation only and "floats" (disables) the IC14, IC15 and IC16 data buses.

DWG 6

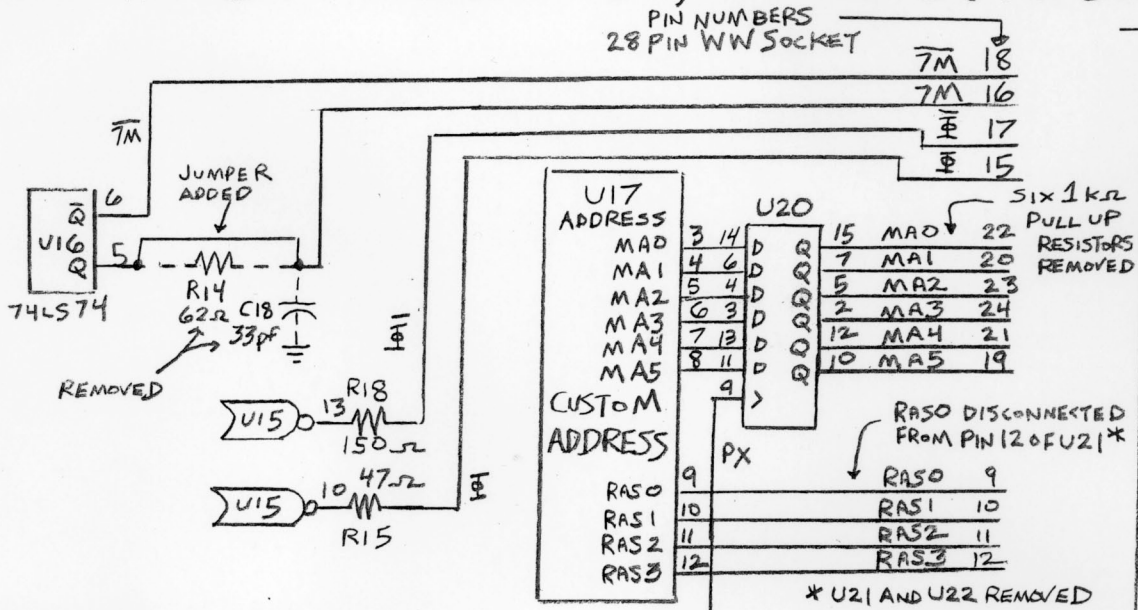
Simplified Video Screen Scan Diagram

The entire TV (video) screen scan circuitry is spread out over drawings 2,3 and 5. DWG 6 lays out the entire scan scheme in this one drawing 6, attempting to simplify the scheme so a user can grasp how the scanning scheme functions. A brief operation description is also included. For more details, reference the doc "A Description of the Bally Professional Arcade Video Hardware and Associated Coin-Operated Hardware" by Anthony J. Miller, which is archived on the Bally Alley website. This doc details the screen scan operation for the coin-op arcade Seawolf II. The scheme in DWG 6 is a variation of the scan scheme used in the DataMax UV-1R computer, which is documented on the Bally Alley website in MCM Design's original hi-res upgrade package 3. The original hi-res upgrade by MCM Design utilized dynamic RAM (DRAM) for it's hi-res screen RAM scheme.

Bye.

MCM

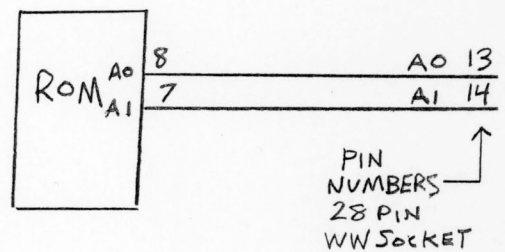
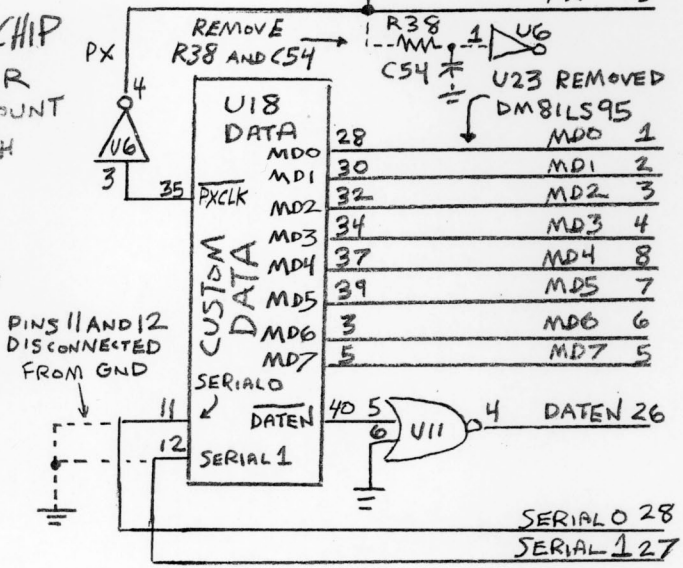
MODIFIED HI-RES MOTHER BOARD, MOUNTED 28 PIN SOCKET WIRING



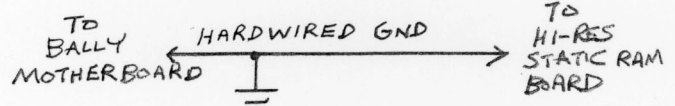
PRIMARY MODIFICATIONS
 REMOVE DRAM CHIPS, U23 CHIP
 MOVE POWER RESISTOR R1 OVER AN INCH TO ALLOW ROOM TO MOUNT 28 PIN WIRE WRAP SOCKET WITH CLIPPED WRAPPING POSTS.

REMOVE CUSTOM DATA CHIP
 SERIAL 0 AND SERIAL 1 LINES FROM GROUND.

OTHER MODIFICATIONS SHOWN MAY NOT BE NECESSARY. MODIFY TO SUIT PROPER TIMING SIGNALS.

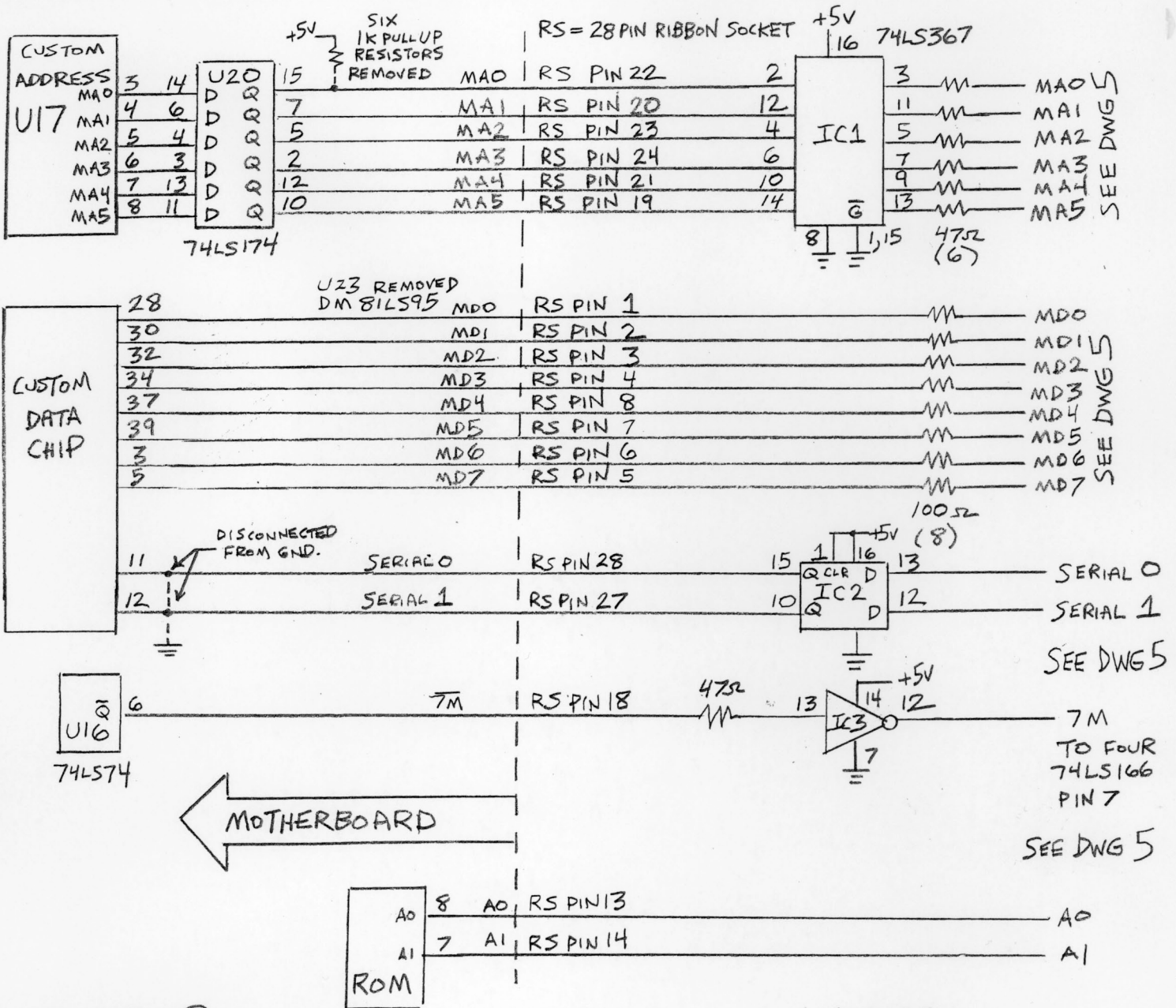


28 PIN WIRE WRAP SOCKET (MOUNTED ON MOTHERBOARD)
 28 PIN DUAL IN-LINE RIBBON CABLE CONNECTION TO HI-RES RAM BOARD.
 TAP 28 LINES TO MOTHERBOARD USING #30 WRAPPING WIRE.
 SOLDER ONE WIRE TO BOARD, OTHER END WRAPPED TO SOCKET.
 USE 20W MAX SOLDERING IRON WITH SHARP POINTED TIP.



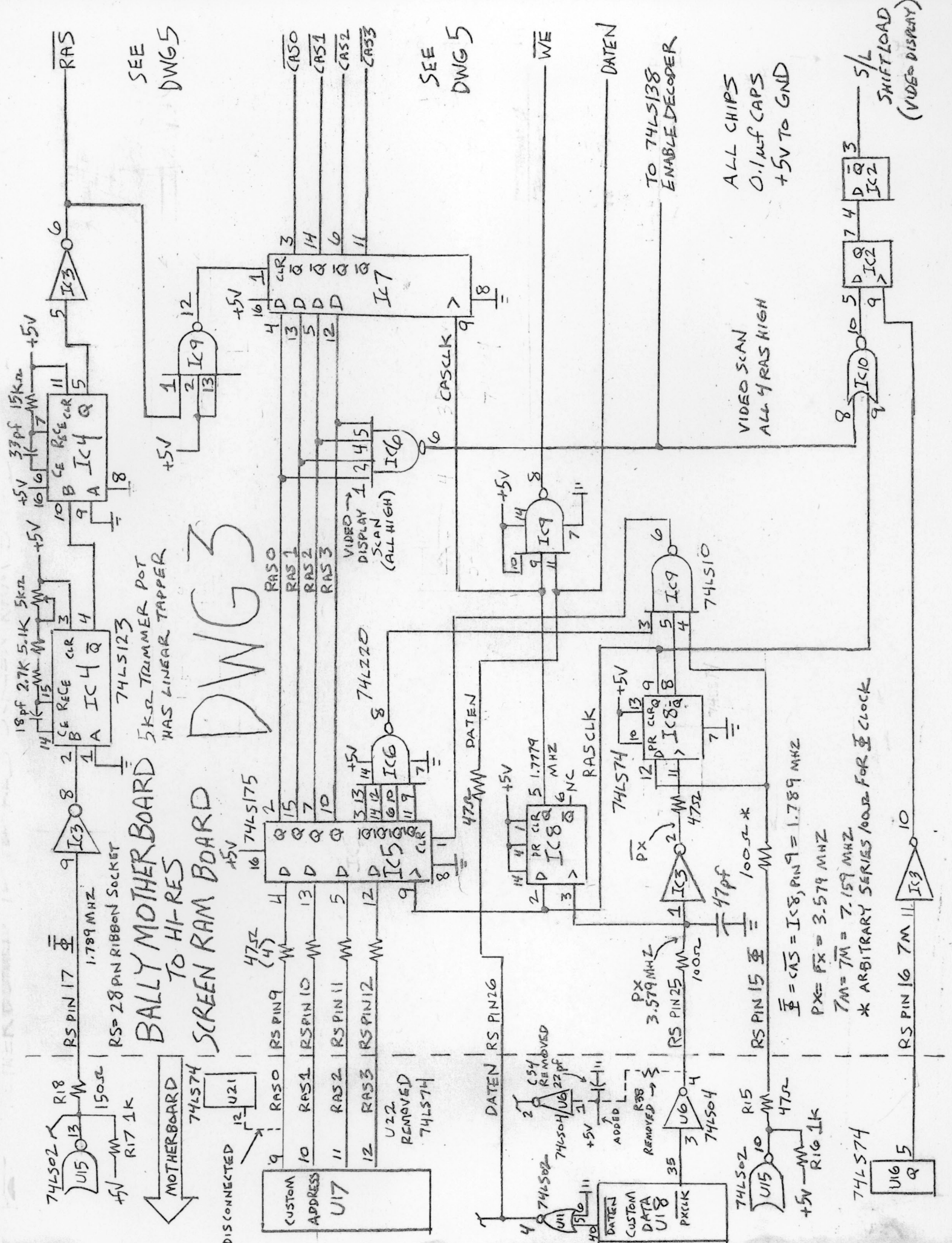
DWG 1

BALLY MOTHER BOARD TO HI-RES SCREEN RAM BOARD



DWG 2

ALL CHIPS
0.1μf CAPS
+5V TO GND



SEE DWG 5

SEE DWG 5

TO 74LS138 ENABLE DECODER

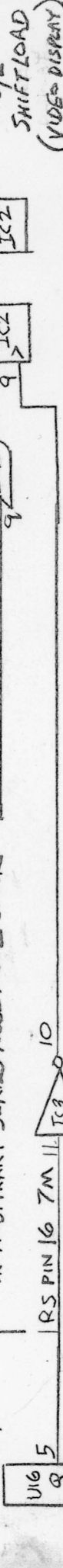
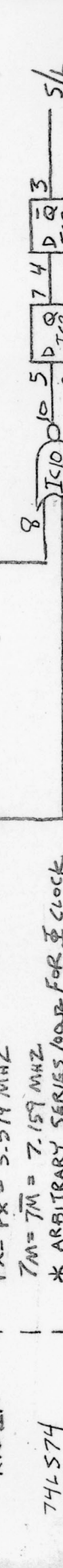
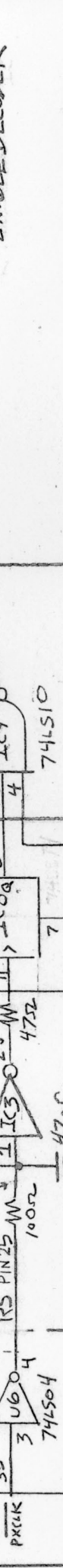
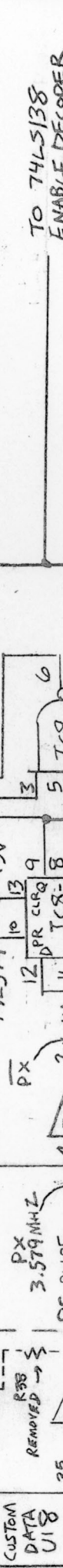
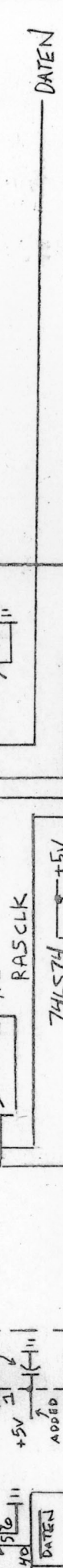
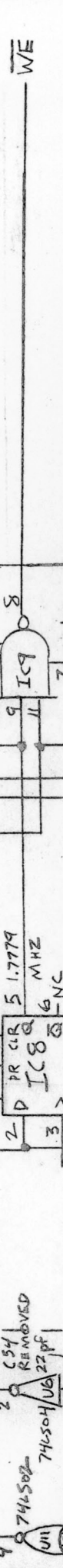
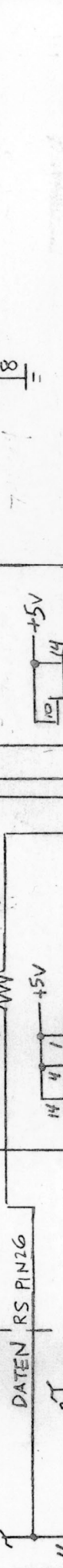
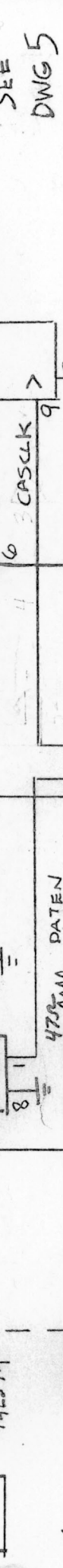
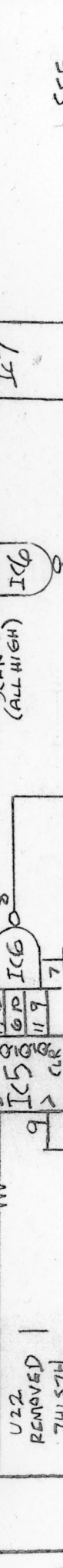
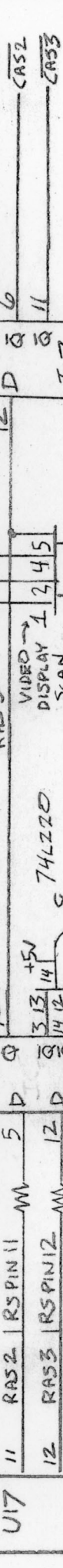
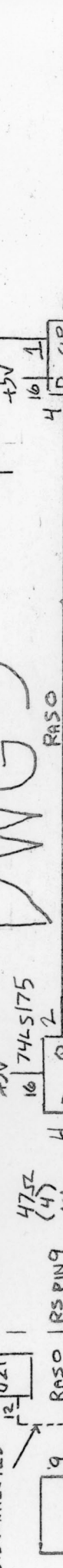
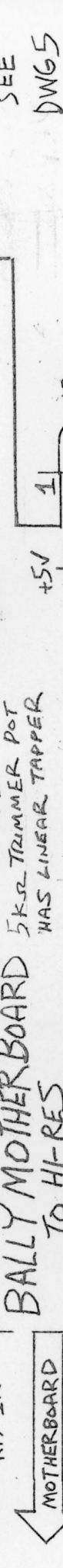
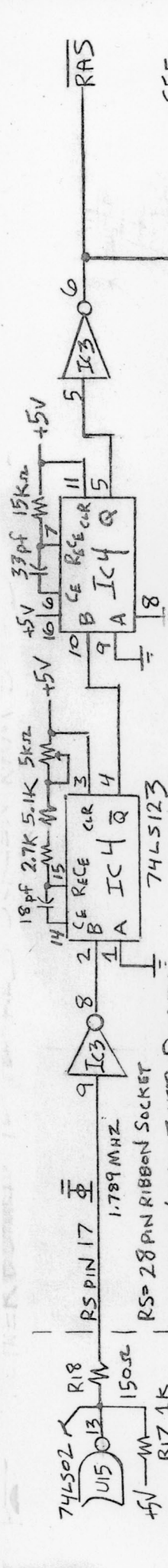
ALL CHIPS 0.1µf CAPS +5V TO GND

VIDEO SCAN ALL 4 RAS HIGH

SHIFTLOAD (VIDEO DISPLAY)

BALLY MOTHERBOARD TO HI-RES SCREEN RAM BOARD

DWG 3



74LS02 U15 13 150Ω R18 150Ω R17 1K MOTHERBOARD 74LS74 U21 DISCONNECTED 74LS174 U17 CUSTOM ADDRESS 74LS175 U18 CUSTOM DATA 74LS176 U19 74LS177 U20 74LS178 U21 74LS179 U22 REMOVED 74LS180 U23 74LS181 U24 74LS182 U25 74LS183 U26 74LS184 U27 74LS185 U28 74LS186 U29 74LS187 U30 74LS188 U31 74LS189 U32 74LS190 U33 74LS191 U34 74LS192 U35 74LS193 U36 74LS194 U37 74LS195 U38 74LS196 U39 74LS197 U40 74LS198 U41 74LS199 U42 74LS200 U43 74LS201 U44 74LS202 U45 74LS203 U46 74LS204 U47 74LS205 U48 74LS206 U49 74LS207 U50 74LS208 U51 74LS209 U52 74LS210 U53 74LS211 U54 74LS212 U55 74LS213 U56 74LS214 U57 74LS215 U58 74LS216 U59 74LS217 U60 74LS218 U61 74LS219 U62 74LS220 U63 74LS221 U64 74LS222 U65 74LS223 U66 74LS224 U67 74LS225 U68 74LS226 U69 74LS227 U70 74LS228 U71 74LS229 U72 74LS230 U73 74LS231 U74 74LS232 U75 74LS233 U76 74LS234 U77 74LS235 U78 74LS236 U79 74LS237 U80 74LS238 U81 74LS239 U82 74LS240 U83 74LS241 U84 74LS242 U85 74LS243 U86 74LS244 U87 74LS245 U88 74LS246 U89 74LS247 U90 74LS248 U91 74LS249 U92 74LS250 U93 74LS251 U94 74LS252 U95 74LS253 U96 74LS254 U97 74LS255 U98 74LS256 U99 74LS257 U100 74LS258 U101 74LS259 U102 74LS260 U103 74LS261 U104 74LS262 U105 74LS263 U106 74LS264 U107 74LS265 U108 74LS266 U109 74LS267 U110 74LS268 U111 74LS269 U112 74LS270 U113 74LS271 U114 74LS272 U115 74LS273 U116 74LS274 U117 74LS275 U118 74LS276 U119 74LS277 U120 74LS278 U121 74LS279 U122 74LS280 U123 74LS281 U124 74LS282 U125 74LS283 U126 74LS284 U127 74LS285 U128 74LS286 U129 74LS287 U130 74LS288 U131 74LS289 U132 74LS290 U133 74LS291 U134 74LS292 U135 74LS293 U136 74LS294 U137 74LS295 U138 74LS296 U139 74LS297 U140 74LS298 U141 74LS299 U142 74LS300 U143 74LS301 U144 74LS302 U145 74LS303 U146 74LS304 U147 74LS305 U148 74LS306 U149 74LS307 U150 74LS308 U151 74LS309 U152 74LS310 U153 74LS311 U154 74LS312 U155 74LS313 U156 74LS314 U157 74LS315 U158 74LS316 U159 74LS317 U160 74LS318 U161 74LS319 U162 74LS320 U163 74LS321 U164 74LS322 U165 74LS323 U166 74LS324 U167 74LS325 U168 74LS326 U169 74LS327 U170 74LS328 U171 74LS329 U172 74LS330 U173 74LS331 U174 74LS332 U175 74LS333 U176 74LS334 U177 74LS335 U178 74LS336 U179 74LS337 U180 74LS338 U181 74LS339 U182 74LS340 U183 74LS341 U184 74LS342 U185 74LS343 U186 74LS344 U187 74LS345 U188 74LS346 U189 74LS347 U190 74LS348 U191 74LS349 U192 74LS350 U193 74LS351 U194 74LS352 U195 74LS353 U196 74LS354 U197 74LS355 U198 74LS356 U199 74LS357 U200 74LS358 U201 74LS359 U202 74LS360 U203 74LS361 U204 74LS362 U205 74LS363 U206 74LS364 U207 74LS365 U208 74LS366 U209 74LS367 U210 74LS368 U211 74LS369 U212 74LS370 U213 74LS371 U214 74LS372 U215 74LS373 U216 74LS374 U217 74LS375 U218 74LS376 U219 74LS377 U220 74LS378 U221 74LS379 U222 74LS380 U223 74LS381 U224 74LS382 U225 74LS383 U226 74LS384 U227 74LS385 U228 74LS386 U229 74LS387 U230 74LS388 U231 74LS389 U232 74LS390 U233 74LS391 U234 74LS392 U235 74LS393 U236 74LS394 U237 74LS395 U238 74LS396 U239 74LS397 U240 74LS398 U241 74LS399 U242 74LS400 U243 74LS401 U244 74LS402 U245 74LS403 U246 74LS404 U247 74LS405 U248 74LS406 U249 74LS407 U250 74LS408 U251 74LS409 U252 74LS410 U253 74LS411 U254 74LS412 U255 74LS413 U256 74LS414 U257 74LS415 U258 74LS416 U259 74LS417 U260 74LS418 U261 74LS419 U262 74LS420 U263 74LS421 U264 74LS422 U265 74LS423 U266 74LS424 U267 74LS425 U268 74LS426 U269 74LS427 U270 74LS428 U271 74LS429 U272 74LS430 U273 74LS431 U274 74LS432 U275 74LS433 U276 74LS434 U277 74LS435 U278 74LS436 U279 74LS437 U280 74LS438 U281 74LS439 U282 74LS440 U283 74LS441 U284 74LS442 U285 74LS443 U286 74LS444 U287 74LS445 U288 74LS446 U289 74LS447 U290 74LS448 U291 74LS449 U292 74LS450 U293 74LS451 U294 74LS452 U295 74LS453 U296 74LS454 U297 74LS455 U298 74LS456 U299 74LS457 U300 74LS458 U301 74LS459 U302 74LS460 U303 74LS461 U304 74LS462 U3

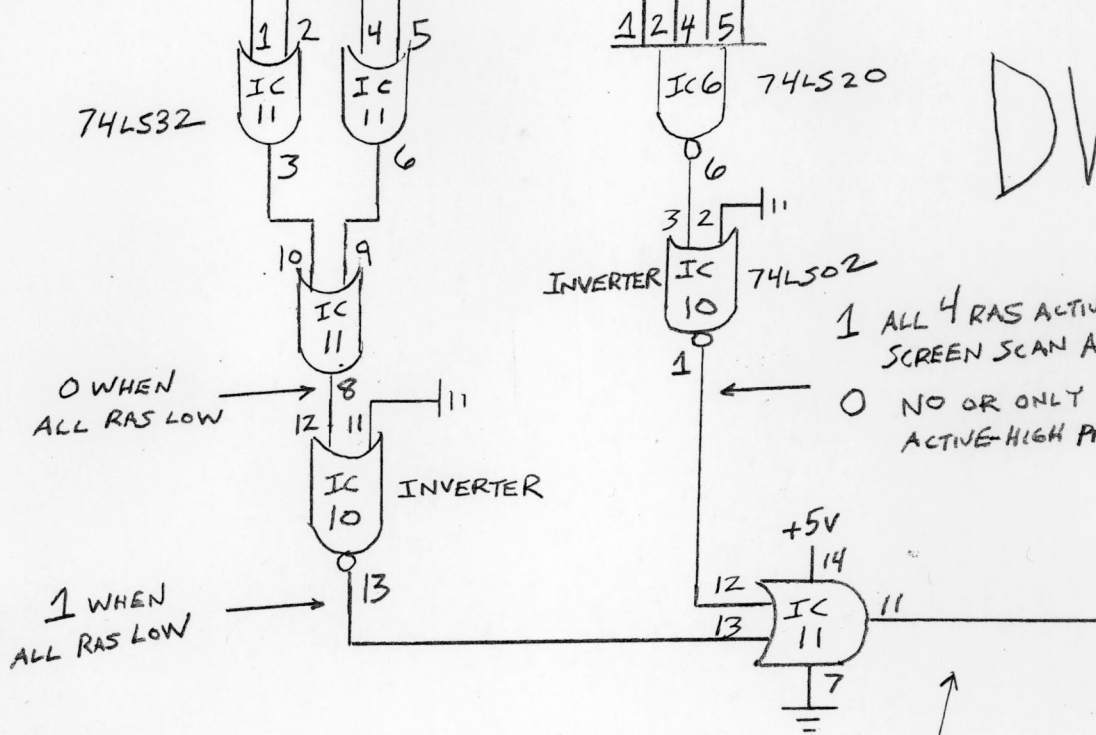
74LS138 ENABLE DECODER

ENABLE ONLY WHEN A SINGLE R/W RAS IS ACTIVE-HIGH

SEE DWG 3
Q OUTPUTS
FROM IC 5

RAS 0
RAS 1
RAS 2
RAS 3

TO IC 7
DATA INPUTS
SEE DWG 3



DWG 4

- 1 ALL 4 RAS ACTIVE-HIGH
SCREEN SCAN ACTIVE
- 0 NO OR ONLY 1 RAS
ACTIVE-HIGH PRESENT

SEE DWG 5
IC 12
TO 74LS138, PIN 4
ACTIVE LOW
ACTIVE MEM R/W ONLY

- NOTES:
- | | | |
|-------|------------------|---|
| RAS 0 | ENABLES RAM BANK | 0 |
| RAS 1 | | 1 |
| RAS 2 | | 2 |
| RAS 3 | | 3 |

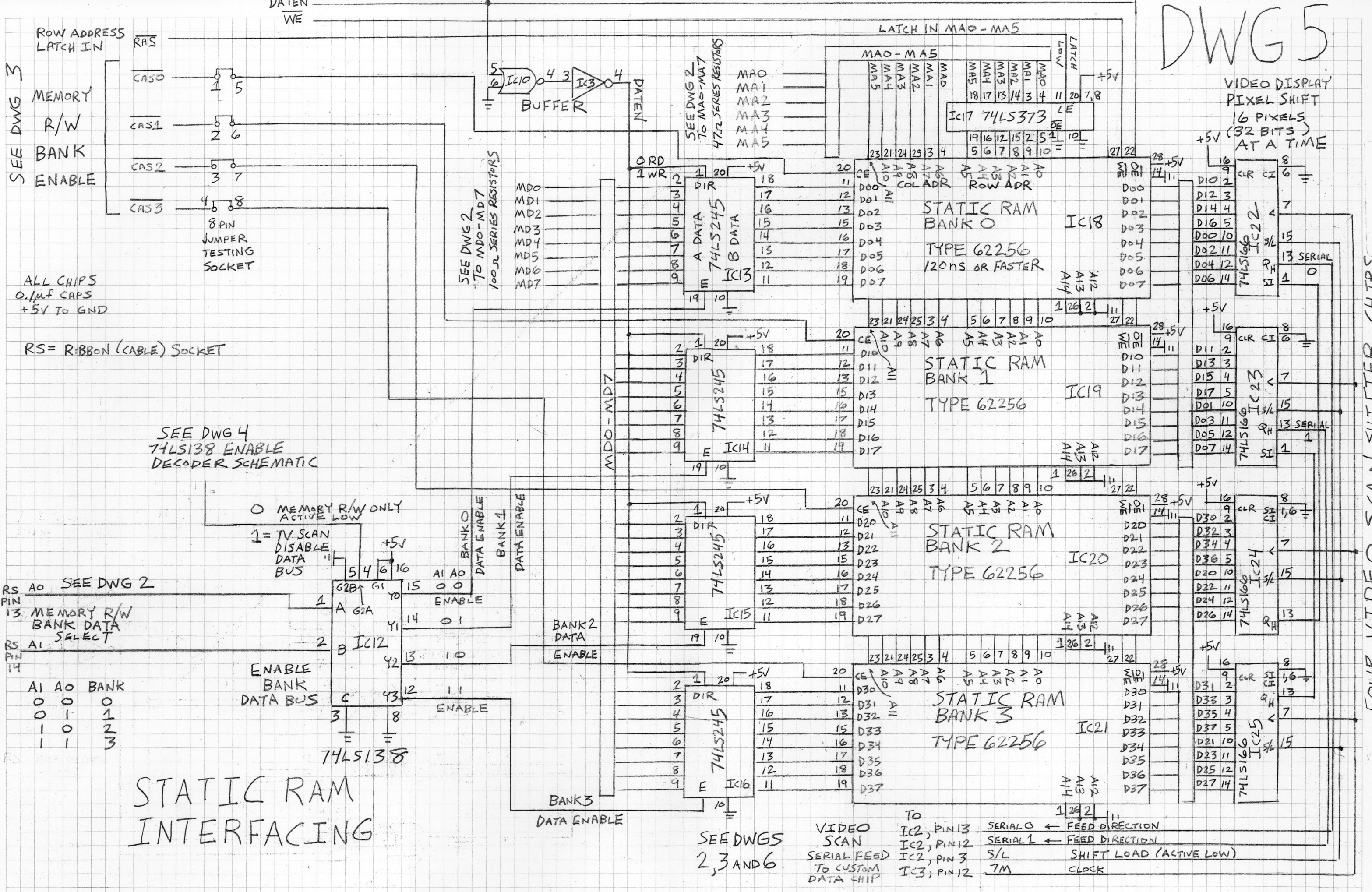
ONE ACTIVE-HIGH RAS SELECTS
SPECIFIC BANK FOR A MEMORY R/W.

ALL 4 RAS LINES ARE ACTIVE-HIGH
SIMULTANEOUSLY FOR A SCREEN SCAN,
4 BYTES (16 PIXELS) ARE SCANNED AT ONE TIME,
LOADED INTO FOUR 74LS166 CHIPS AND
SHIFTED SERIALLY INTO CUSTOM DATA CHIP
USING THE TWO SERIAL 0 AND SERIAL 1 LINES.

- 1 DISABLE 74LS138
ALL RAS HIGH (SCREEN SCAN)
OR
ALL RAS LOW (INACTIVE)
- 0 ENABLE 74LS138
ACTIVE ONLY WHEN A
SINGLE R/W ACTIVE-HIGH PULSE
IS PRESENT.

ALL CHIPS
0.1µf CAPS
+5V TO GND

DWG 5



SEE DWG 3
MEMORY R/W BANK ENABLE

ALL CHIPS 0.1μF CAPS +5V TO GND

RS = RIBBON (CABLE) SOCKET

SEE DWG 4 74LS138 ENABLE DECODER SCHEMATIC

0 MEMORY R/W ONLY ACTIVE LOW
1 TV SCAN DISABLE DATA BUS

RS A0 SEE DWG 2
13 MEMORY R/W BANK DATA SELECT
RS A1

A1	A0	BANK
0	0	0
0	1	1
1	0	2
1	1	3

STATIC RAM INTERFACING

SEE DWGS 2, 3 AND 6

VIDEO SCAN SERIAL FEED TO CUSTOM DATA CHIP

To	IC2, PIN 13	SERIAL0	← FEED DIRECTION
IC2, PIN 12	SERIAL1	← FEED DIRECTION	
IC2, PIN 3	S/L	SHIFT LOAD (ACTIVE LOW)	
IC3, PIN 12	7M	CLOCK	

VIDEO DISPLAY PIXEL SHIFT 16 PIXELS (32 BITS) AT A TIME

FOUR VIDEO SCAN SHIFTER CHIPS

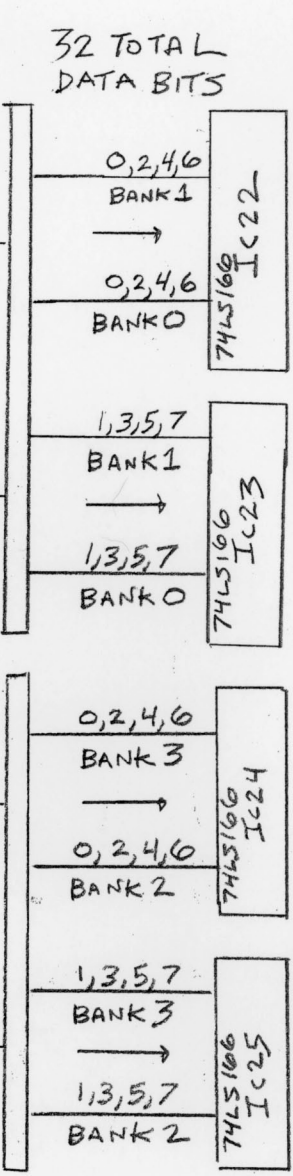
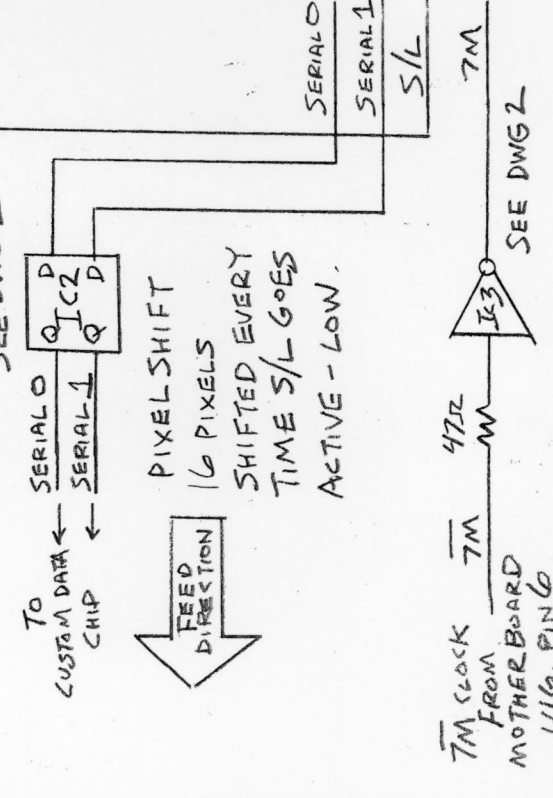
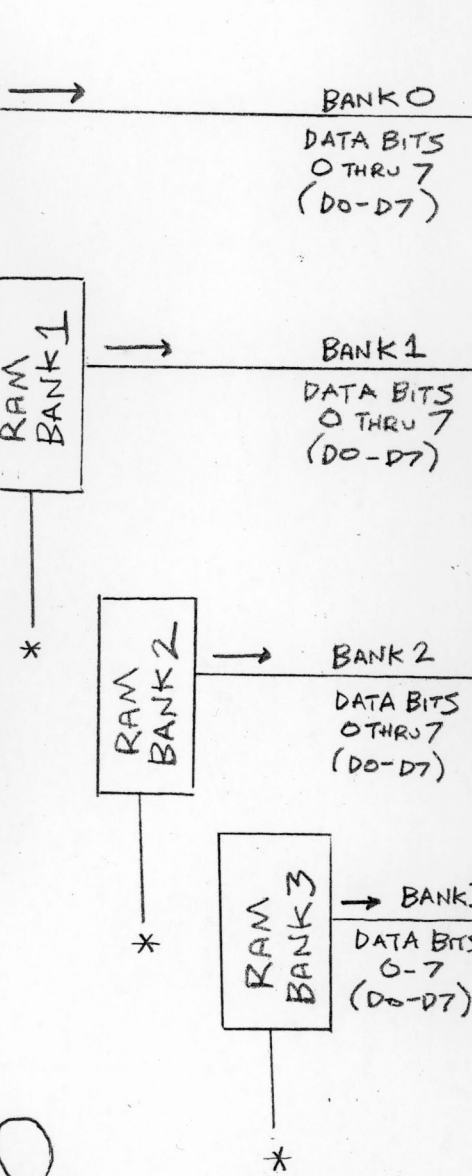
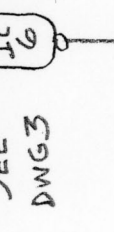
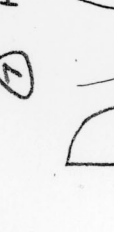
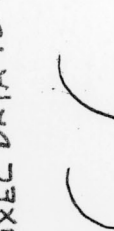
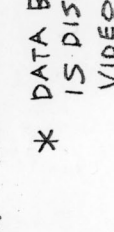
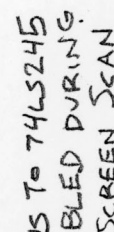
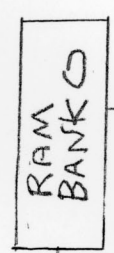
SIMPLIFIED VIDEO SCREEN SCAN DIAGRAM (SCAN ACTS LIKE A MEMORY READ)

- 1 ALL FOUR RAS LINES GO ACTIVE-HIGH SIMULTANEOUSLY.
- 2 ALL FOUR 74LS245 CHIPS ARE DISABLED (CUSTOM CHIP DATA BUS IS DISCONNECTED).
- 3 CUSTOM ADDRESS CHIP SENDS ROW AND COLUMN ADDRESSES TO RAM.
- 4 ONE BYTE IN EACH RAM BANK IS READ SIMULTANEOUSLY.
- 5 READ DATA (4 BYTES, 32 BITS, 16 PIXELS) APPEARS AT 4 SHIFTERS IC22-IC25 INPUTS.
- 6 SHIFT LOAD (S/L) GOES ACTIVE-LOW (TIME TO SHIFT THE 16 PIXELS).
- 7 PIXEL DATA IS SHIFTED TO CUSTOM DATA CHIP SERIALLY 2 BITS AT A TIME.

DWG 6



SEE DWG 3



FOR WIRING TO FOUR 74LS166 SEE STATIC RAM INTERFACING SCHEMATIC DWG 5

7M CLOCK FROM MOTHER BOARD U16, PIN 16