Hi-Res Static Screen Ram Schematics Overview
By Michael Matte
September 20, 2019

Subject: Re: Hi-Res Static RAM Project Update
From: MCM Design
Date: 9/20/2019, 5:37 PM
To: Adam Trionfo

The DWGs 1 thru 6 are finalized. You can post/forward these first 6 drawings as desired. DWG 5 as shown is for hi-res operation only with no multi-paging. The upcoming, additional drawings will be submitted to you as options to the original hi-res static screen RAM scheme (DWG 5). A user interested in building the new hi-res static screen RAM scheme can choose what option he/she wants to add on. There WILL be an option drawing for someone that just wants to operate the static screen RAM in low or hi-res with NO multi-paging. An option drawing will include and indicate any rewire necessary to DWG 4 or 5.

I just finished writing my overview. I will send it to you in a few minutes after I proof read it.

Bye.
MCM

Subject: Hi-Res Static RAM Project Update
From: MCM Design
Date: 9/20/2019, 5:54 PM

HI-RES STATIC SCREEN RAM SCHEMATICS OVERVIEW

DWG 1
Modified Hi-Res Motherboard, Mounted 28 Pin Socket Wiring
Details the necessary motherboard modifications for hi-res operation. Includes 28 wiring lines from the motherboard to the 28 pin WW socket mounted on the motherboard.

DWG 2
Bally Motherboard To Hi-Res Screen RAM Board
Shows some of the necessary interfacing from the 28 pin ribbon cable connection on the motherboard to the static screen RAM board scheme and the TV display scan circuitry detailed in DWG 5.

DWG 3
Bally Motherboard To Hi-Res Screen RAM Board
Shows additional interfacing and timing circuitry. Reference above DWG 2 description.

DWG 4
74LS138 Enabler Decoder
Details the 74LS138 decoder for proper operation of the Z80 screen RAM read/write data bus and the TV display scan 32 bit read (scan) data bus.

DWG 5

Static Screen RAM Interfacing
Details interfacing and all connections to the 4 banks of static screen RAM. Includes connections to the four 74LS166 TV display scan serial shifter chips.

User Notes

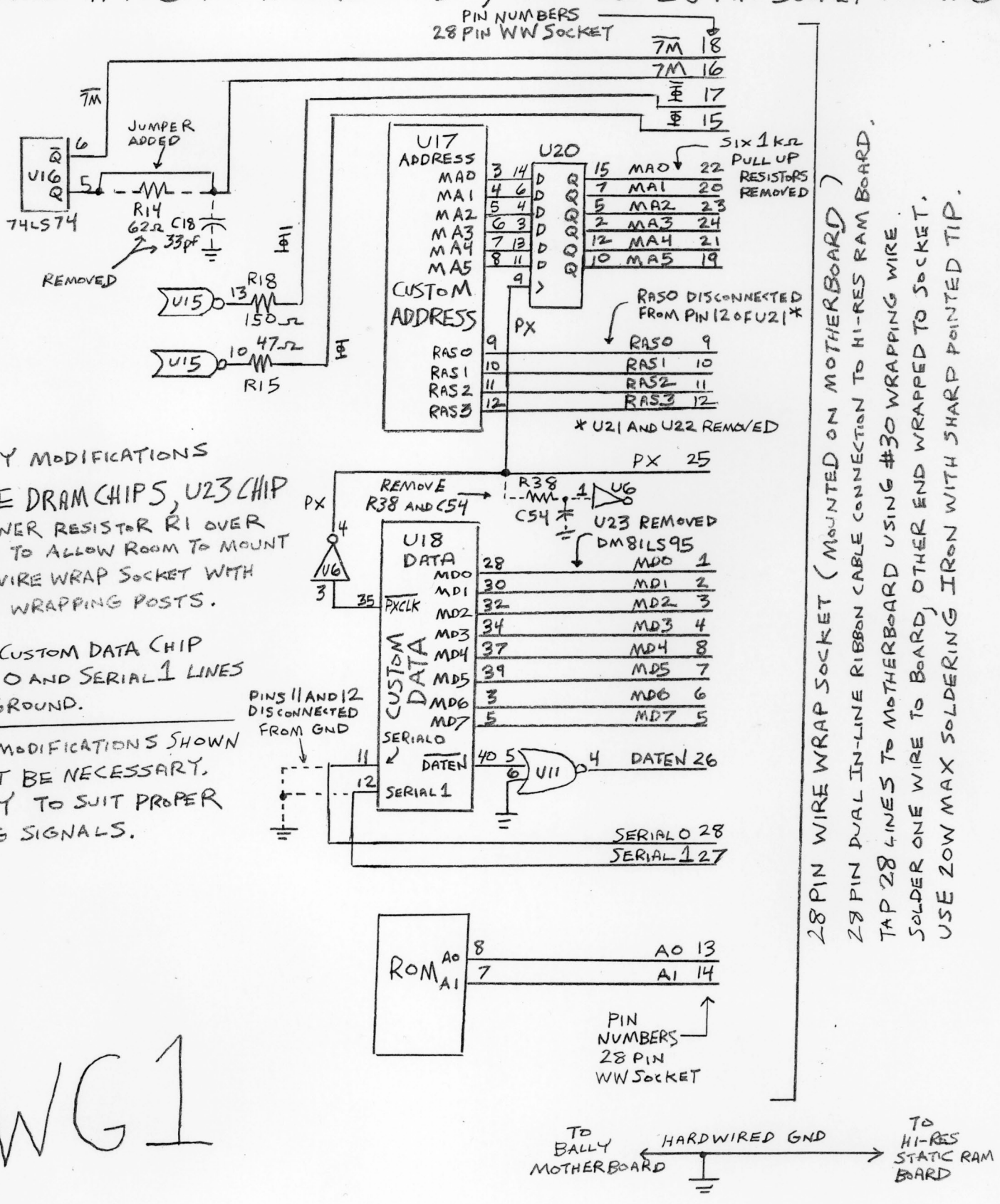
1. Check your static RAM pin layout for compatibility with the static RAM pin layout in DWG 5. If your static RAM pin layout is NOT compatible, wire your RAM to suit proper operation (or purchase compatible chips) and revise your version of DWG 5 for future reference.

2. DWG 5 as shown is wired for hi-res operation only with no multi-paging. To manually run this DWG 5 scheme in low-res, remove the IC12 chip 74LS138 from its socket. Add a jumper wire from the socket pin 15 to gnd pin 8. This jumper enables the Bank 0 RAM data bus for low-res operation only and "floats" (disables) the IC14, IC15 and IC16 data buses.

DWG 6
Simplified Video Screen Scan Diagram
The entire TV (video) screen scan circuitry is spread out over drawings 2,3 and 5. DWG 6 lays out the entire scan scheme in this one drawing 6, attempting to simplify the scheme so a user can grasp how the scanning scheme functions. A brief operation description is also included. For more details, reference the doc "A Description of the Bally Professional Arcade Video Hardware and Associated Coin-Operated Hardware" by Anthony J. Miller, which is archived on the Bally Alley website. This doc details the screen scan operation for the coin-op arcade Seawolf II. The scheme in DWG 6 is a variation of the scan scheme used in the DataMax UV-1R computer, which is documented on the Bally Alley website in MCM Design's original hi-res upgrade package 3. The original hi-res upgrade by MCM Design utilized dynamic RAM (DRAM) for it's hi-res screen RAM scheme.

Bye.
MCM

MODIFIED HI-RES MOTHERBOARD, MOUNTED 28 PIN SOCKET WIRING



PRIMARY MODIFICATIONS

REMOVE DRAM CHIPS, U23 CHIP

MOVE POWER RESISTOR R1 OVER AN INCH TO ALLOW ROOM TO MOUNT 28 PIN WIRE WRAP SOCKET WITH CLIPPED WRAPPING POSTS.

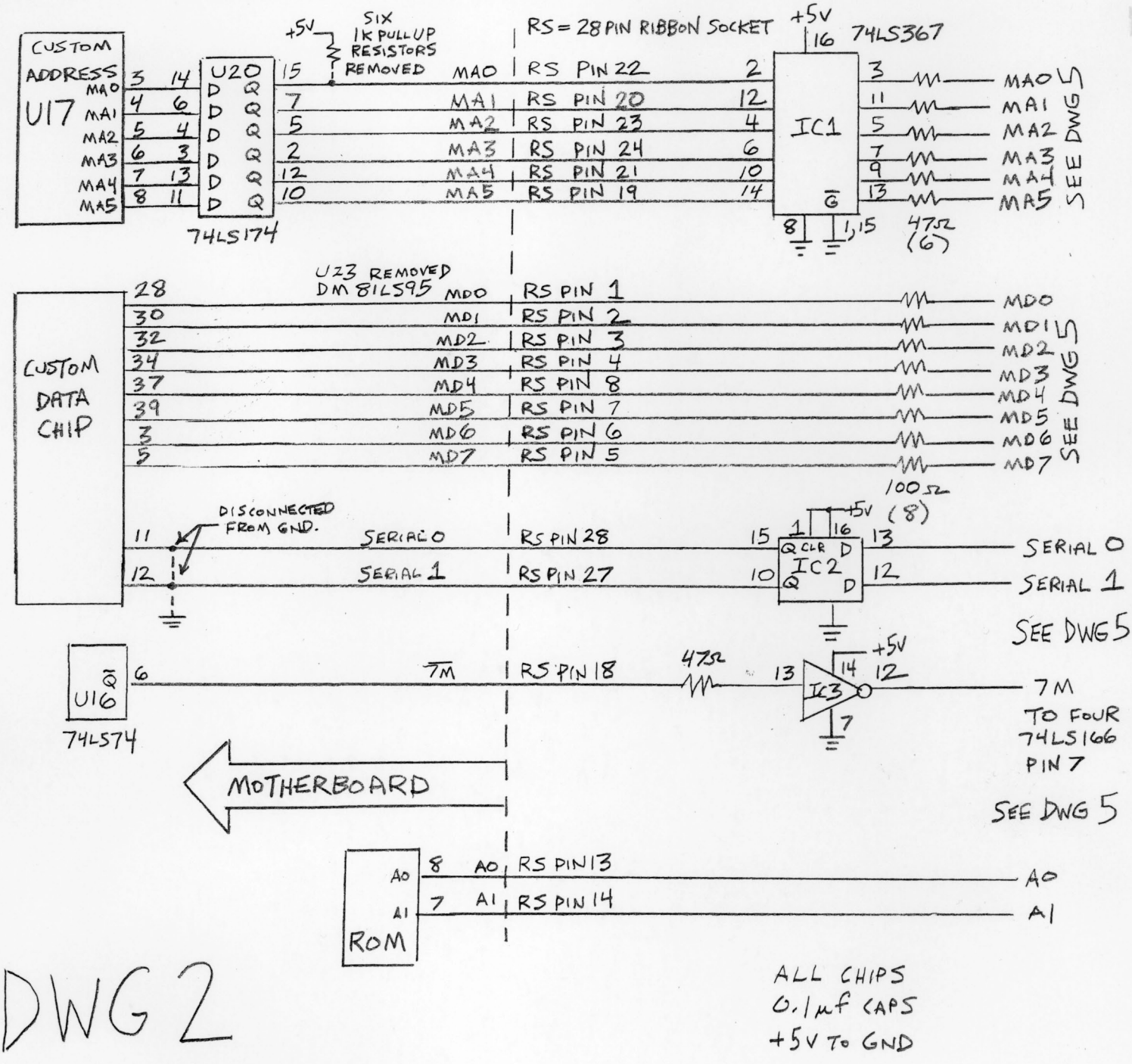
REMOVE CUSTOM DATA CHIP SERIAL 0 AND SERIAL 1 LINES FROM GROUND.

OTHER MODIFICATIONS SHOWN MAY NOT BE NECESSARY. MODIFY TO SUIT PROPER TIMING SIGNALS.

DWG1

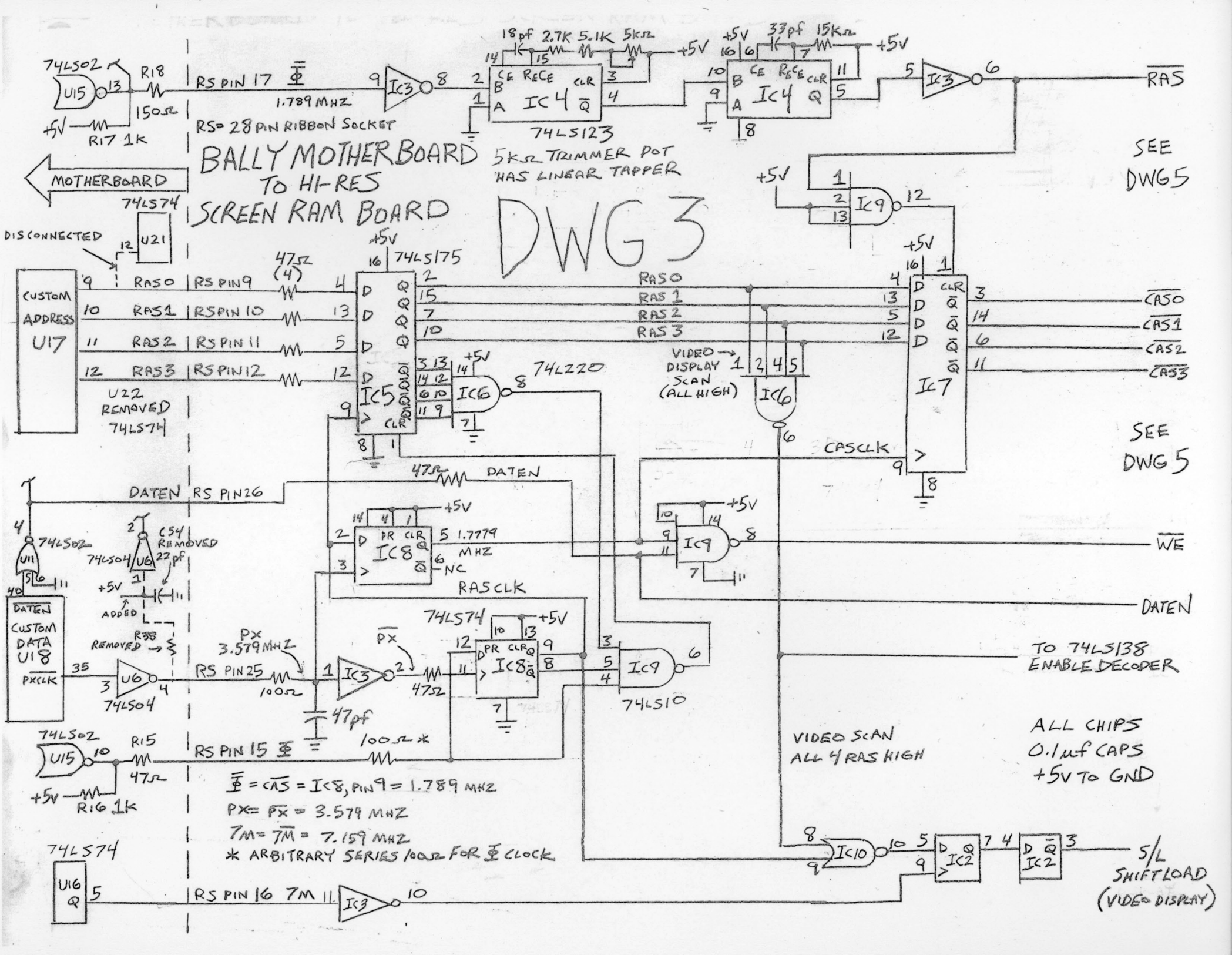
TO BALLY MOTHERBOARD — HARDWIRED GND — TO HI-RES STATIC RAM BOARD

BALLY MOTHERBOARD TO HI-RES SCREEN RAM BOARD



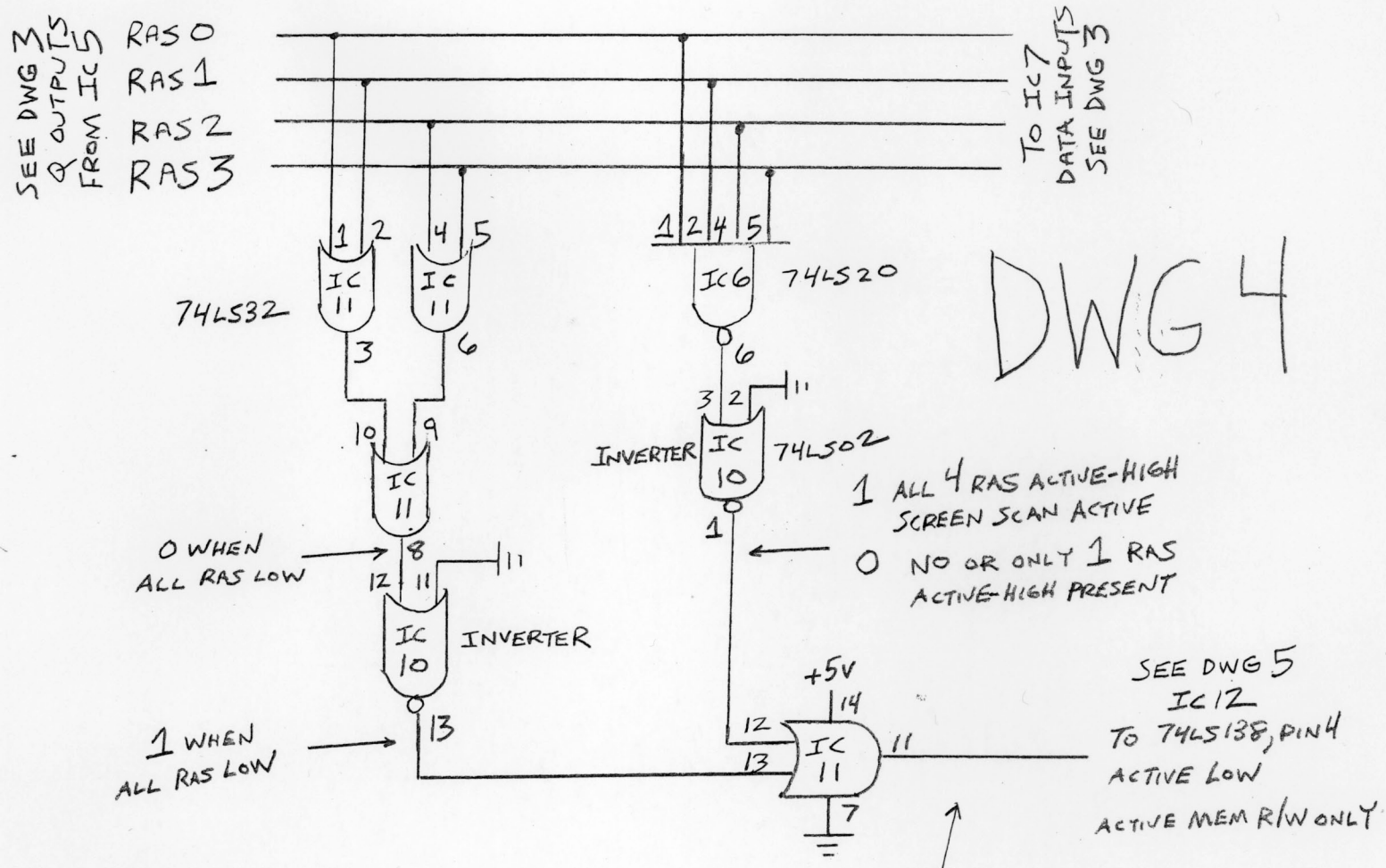
DWG 2

ALL CHIPS
0.1μf CAPS
+5V TO GND


BALLY MOTHERBOARD
TO HI-RES
SCREEN RAM BOARD
DWG3
MOTHERBOARD
RS= 28 PIN RIBBON SOCKET
RS PIN 17 Φ
1.789 MHZ
74LS123
5KΩ TRIMMER POT
HAS LINEAR TAPPER
SEE DWG5
SEE DWG5
74LS74
DISCONNECTED
U22 REMOVED 74LS74
CUSTOM ADDRESS U17
RAS0
RAS1
RAS2
RAS3
RS PIN9
RS PIN10
RS PIN11
RS PIN12
74LS175
74LS220
VIDEO DISPLAY SCAN (ALL HIGH)
CASCLK
CAS0
CAS1
CAS2
CAS3
DATEN
RS PIN26
C54 REMOVED
22pf ADDED
R38 REMOVED
CUSTOM DATA U18
PXCLK
PX 3.579 MHZ
RS PIN25
100Ω
47pf
74LS04
74LS10
RASCLK
1.7779 MHZ
NC
WE
TO 74LS138 ENABLE DECODER
VIDEO SCAN ALL 4 RAS HIGH
ALL CHIPS 0.1μf CAPS +5V TO GND
RS PIN15 Φ
100Ω*
Φ = CAS = IC8, PIN 9 = 1.789 MHZ
PX = PX = 3.579 MHZ
7M = 7M = 7.159 MHZ
* ARBITRARY SERIES 100Ω FOR Φ CLOCK
RS PIN16 7M
S/L SHIFT LOAD (VIDEO DISPLAY)

74LS138 ENABLE DECODER

ENABLE ONLY WHEN A SINGLE R/W RAS IS ACTIVE-HIGH



NOTES: RAS 0 ENABLES RAM BANK 0
RAS 1 — 1
RAS 2 — 2
RAS 3 — 3

ONE ACTIVE-HIGH RAS SELECTS SPECIFIC BANK FOR A MEMORY R/W.

ALL 4 RAS LINES ARE ACTIVE-HIGH SIMULTANEOUSLY FOR A SCREEN SCAN, 4 BYTES (16 PIXELS) ARE SCANNED AT ONE TIME, LOADED INTO FOUR 74LS166 CHIPS AND SHIFTED SERIALLY INTO CUSTOM DATA CHIP USING THE TWO SERIAL 0 AND SERIAL 1 LINES.

1 DISABLE 74LS138
ALL RAS HIGH (SCREEN SCAN)
OR
ALL RAS LOW (INACTIVE)

0 ENABLE 74LS138
ACTIVE ONLY WHEN A SINGLE R/W ACTIVE-HIGH PULSE IS PRESENT.

ALL CHIPS
0.1μf CAPS
+5V TO GND

DWG 5

STATIC RAM INTERFACING

SEE DWG 3

ROW ADDRESS LATCH IN — RAS

MEMORY R/W BANK ENABLE — CAS0, CAS1, CAS2, CAS3

8 PIN JUMPER TESTING SOCKET

ALL CHIPS
0.1µf CAPS
+5V TO GND

RS = RIBBON (CABLE) SOCKET

DATEN
WE

IC10 BUFFER IC3 — DATEN

SEE DWG 2 TO MD0-MD7 100Ω SERIES RESISTORS

SEE DWG 2 TO MA0-MA7 47Ω SERIES RESISTORS

MD0 MD1 MD2 MD3 MD4 MD5 MD6 MD7

MA0 MA1 MA2 MA3 MA4 MA5

ORD
1WR

IC13 74LS245 A DATA B DATA DIR E

IC14 74LS245 DIR E

IC15 74LS245 DIR E

IC16 74LS245 DIR E

LATCH IN MA0-MA5

MA0-MA5 LOW LATCH

IC17 74LS373 LE OE +5V

STATIC RAM BANK 0 TYPE 62256 120ns OR FASTER — IC18

STATIC RAM BANK 1 TYPE 62256 — IC19

STATIC RAM BANK 2 TYPE 62256 — IC20

STATIC RAM BANK 3 TYPE 62256 — IC21

A0-A7 COL ADR
A5 A11 A13 A12 A14 ROW ADR
CE WE OE
D00-D07 / D10-D17 / D20-D27 / D30-D37

VIDEO DISPLAY PIXEL SHIFT
16 PIXELS (32 BITS) AT A TIME

IC22 74LS166 — IC23 74LS166 — IC24 74LS166 — IC25 74LS166
CLR CI S/L RH SI SERIAL 0 SERIAL 1

FOUR VIDEO SCAN SHIFT REGISTER CHIPS

SEE DWG 4
74LS138 ENABLE DECODER SCHEMATIC

0 = MEMORY R/W ONLY ACTIVE LOW
1 = TV SCAN DISABLE DATA BUS

IC12 74LS138 — G2B G2A G1 A B C — Y0 Y1 Y2 Y3

A1 A0 BANK ENABLE
0 0 0
0 1 1
1 0 2
1 1 3

BANK 0 DATA ENABLE
BANK 1 DATA ENABLE
BANK 2 DATA ENABLE
BANK 3 DATA ENABLE

RS PIN 13 A0 — SEE DWG 2 — MEMORY R/W BANK DATA SELECT
RS PIN 14 A1

ENABLE BANK DATA BUS

SEE DWGS 2, 3 AND 6

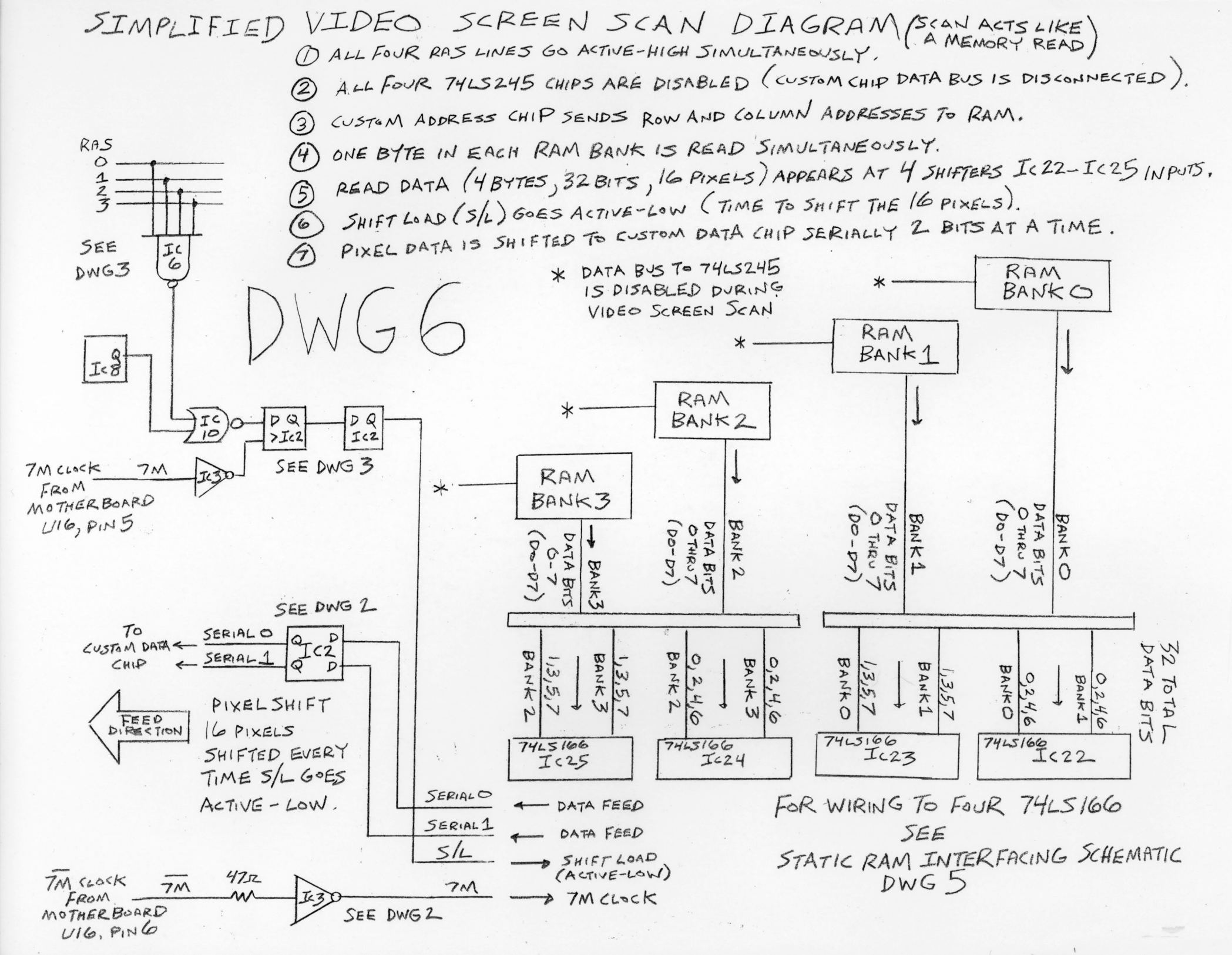
VIDEO SCAN SERIAL FEED TO CUSTOM DATA CHIP

TO IC2, PIN 13	SERIAL 0	← FEED DIRECTION
IC2, PIN 12	SERIAL 1	← FEED DIRECTION
IC2, PIN 3	S/L	SHIFT LOAD (ACTIVE LOW)
IC3, PIN 12	7M	CLOCK

SIMPLIFIED VIDEO SCREEN SCAN DIAGRAM (SCAN ACTS LIKE A MEMORY READ)

1. ALL FOUR RAS LINES GO ACTIVE-HIGH SIMULTANEOUSLY.
2. ALL FOUR 74LS245 CHIPS ARE DISABLED (CUSTOM CHIP DATA BUS IS DISCONNECTED).
3. CUSTOM ADDRESS CHIP SENDS ROW AND COLUMN ADDRESSES TO RAM.
4. ONE BYTE IN EACH RAM BANK IS READ SIMULTANEOUSLY.
5. READ DATA (4 BYTES, 32 BITS, 16 PIXELS) APPEARS AT 4 SHIFTERS IC22–IC25 INPUTS.
6. SHIFT LOAD (S/L) GOES ACTIVE-LOW (TIME TO SHIFT THE 16 PIXELS).
7. PIXEL DATA IS SHIFTED TO CUSTOM DATA CHIP SERIALLY 2 BITS AT A TIME.

DWG 6



FOR WIRING TO FOUR 74LS166 SEE STATIC RAM INTERFACING SCHEMATIC DWG 5